



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Ritsuko Iwasaki

Serial No.: 09/496,421

Group Art Unit: 2815

Filed: February 2, 2000

Examiner: Lee, E.

For: SEMICONDUCTOR DEVICE HAVING AN IMPROVED LAYOUT PATTERN OF  
PAIR TRANSISTORS

Honorable Assistant Commissioner of Patents  
Washington, D.C. 20231

#14/C  
10/22/2  
Suler  
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OCT 18 2002  
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PRELIMINARY AMENDMENT

Sir:

Prior to further examination on the merits and calculation of the filing fee and concurrently with the Request for Continued Examination (RCE) filed herewith, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 6-9 without prejudice or disclaimer.

Please add the following new claims.

- CI
- 1 -- 26. A semiconductor device including first and second transistors formed on a
  - 2 semiconductor chip, each having a terminal commonly connected to a node, said device
  - 3 comprising:
  - 4 a main line of a first gate electrode layer of said first transistor extending in a first
  - 5 direction;
  - 6 two branches branching substantially perpendicularly from said main line of said first
  - 7 gate electrode layer, said two branches extending in a second direction;
  - 8 a first diffusion layer of said first transistor coupled to a first contact hole;



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**EXCESS CLAIM FEE PAYMENT LETTER**

Sir:

Transmitted herewith is an amendment in the above-identified application. The fee has been calculated and is transmitted as shown below.

	<u>AFTER AMENDMENT</u>	<u>PREV. PAID FOR</u>	<u>EXTRA CLAIMS PRESENT</u>	<u>RATE</u>	<u>FEE DUE</u>
Total Claims	22 -	22	= 0	x \$18.00	\$ 00.00
Indep. Claims	5 -	4	= 1	x \$84.00	\$ 84.00
<b>TOTAL ADDITIONAL FEE FOR THIS AMENDMENT</b>					<b>\$ 84.00</b>

A check in the amount of \$ 84.00 is herewith enclosed to cover the excess claim fees. A duplicate copy of this sheet is enclosed.

Date:

10/15/02

Respectfully Submitted,

Sean M. McGinn  
Reg. No. 34,386

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